Application Note:
HFDN-1.0
Rev 0; 5/00

Disabling the Channel-Assignment Feature of the MAX3831

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I. Overview

The MAX3831 Mux/Demux has a channel assignment feature that allows it to properly assign the outputs to the correct channels. When enabled this feature only works with framed SDH/SONET data signals. This design note discusses how to disable the channel assignment feature for those applications where the user wants to perform the channel assignment downstream or for non-SDH/SONET applications.

II. Description of the Channel Assignment Feature

Channel assignment is achieved by watching for the byte sequence A1 A1 A2 A2, which is common to all SDH/SONET headers. The MAX3831 inverts channel 4 at the multiplexer and then inverts channel 4 again at the demultiplexer. If the channels are properly assigned, the inversion at the channel 4 output will cancel the inversion on the channel 4 input, and all polarities will be correct. (See Table 1) In any other order of channel assignment, the channel 4 output will contain an inverted data stream (see Figure 1) and the A1 A1 A2 A2 framing pattern will not be found. If after 250µs a framing pattern has not been located, the frame detector will automatically 'roll' the channel assignment and the searching will continue. This searching and rolling will continue indefinitely until a framing pattern is found.

			Receiver Output Data			
	Transmitter Input Data	Transmitted Serial Data	Case #1	Case #2	Case #3	Case #4 (Proper Assignment)
Channel 1	$D1$	$D1$	$D2$	$D3$	$\overline{D4}$	$D1$
Channel 2	$D2$	$D2$	$D3$	$\overline{D4}$	$D1$	$D2$
Channel 3	$D3$	$D3$	$\overline{D4}$	$D1$	$D2$	$D3$
Channel 4	$D4$	$\overline{D4}$	$\overline{D1}$	$\overline{D2}$	$\overline{D3}$	$D4$

Table 1. Possible data output alignments at the demultiplexer.

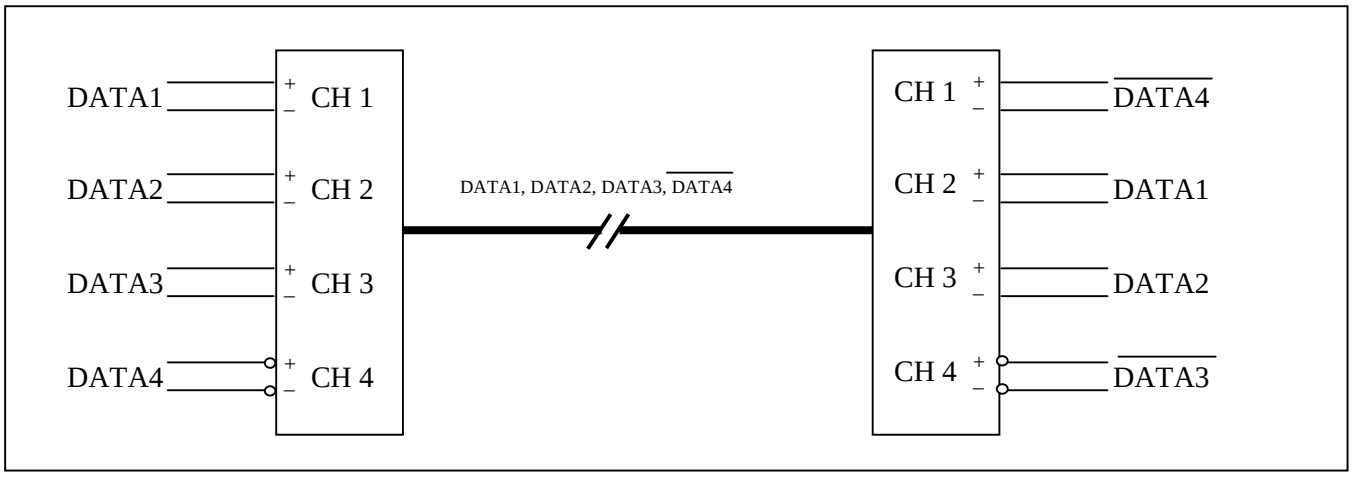


Figure 1. Frame detection/channel assignment disabled, with inverted outputs at demultiplexer.

III. How to Disable Channel Assignment

To disable the channel assignment feature of the MAX3831, the reset-frame pin ($\overline{RSETFR}$) must be held at ground. This will stop the automatic roll associated with the channel assignment feature. The outputs will not be aligned, but they will always be in sequencial order. (For example, DATA1 will always be one channel before DATA2.) This means that once the location of one of the channels is determined, the location of all other channels can be inferred.

IV. What About the Inversions at the Multiplexer and Demultiplexer?

In order to avoid inverted outputs when the frame detection is disabled, (see Table 1 and Figure 1), the two inversions on channel 4 need to be addressed. By externally inverting channel 4 at both the input and the output, the effects of the on-chip inversion will be negated. The external inversion can be achieved by using logic inverters, but at the cost of excessive channel-to-channel skew. A simpler solution is to swap the polarity of the data lines at the input and outputs of channel 4. This solution is lower-cost, and doesn't add additional channel-to-channel skew. An illustration of this application is shown in Figure 2.

V. Timing requirements to ensure data alignment

The MAX3831 was designed to multiplex and demultiplex four independent channels of OC-12 SDH/SONET data. Because all four parallel input channels are assumed to be independent of one another and of RCLKI, the MAX3831 is designed so that there are no setup and hold time requirements. However, if no attention is paid to timing, the order in which the parallel channels are multiplexed is indeterminate. As an example, suppose:

PDI1 = A0, A1, A2
PDI2 = B0, B1, B2
PDI3 = C0, C1, C2
PDI4 = D0, D1, D2

are applied to the parallel inputs with no particular timing.

The serial output may be:

SDO = A0, B0, C1, D0, A1, B1, C2, D1, …

When all four parallel channels are coming from the same source, it is important that the elastic store not change the order in which the parallel channels are multiplexed. If it is desired that the serial data be in order (i.e. SDO = A0, B0, C0, D0, A1, B1, …) then certain timing requirements must be met. The convention used here is a common setup and hold timing diagram even though these aren't strictly setup and hold times. These times only represent the

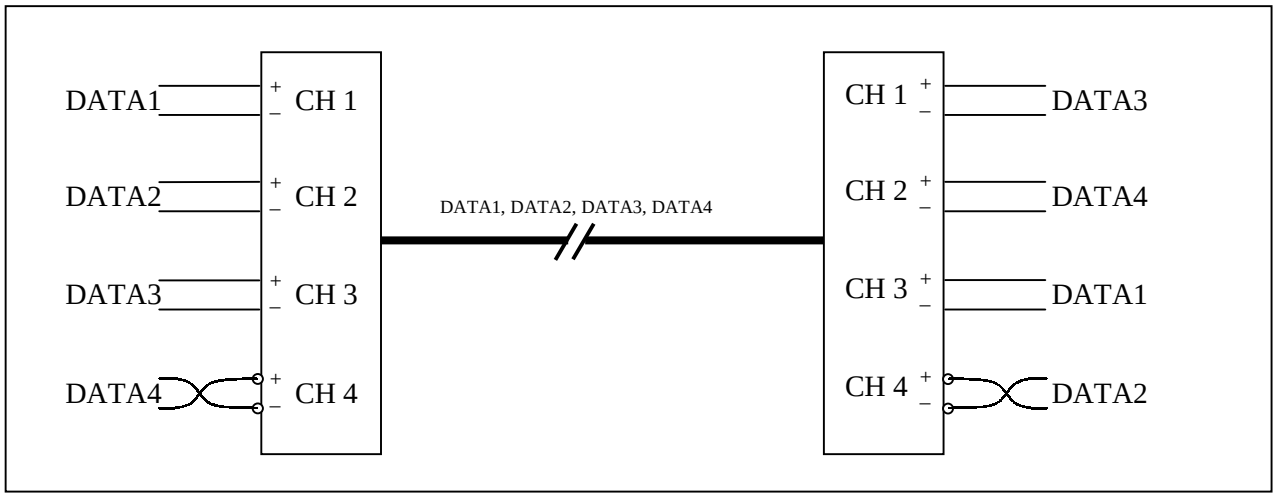


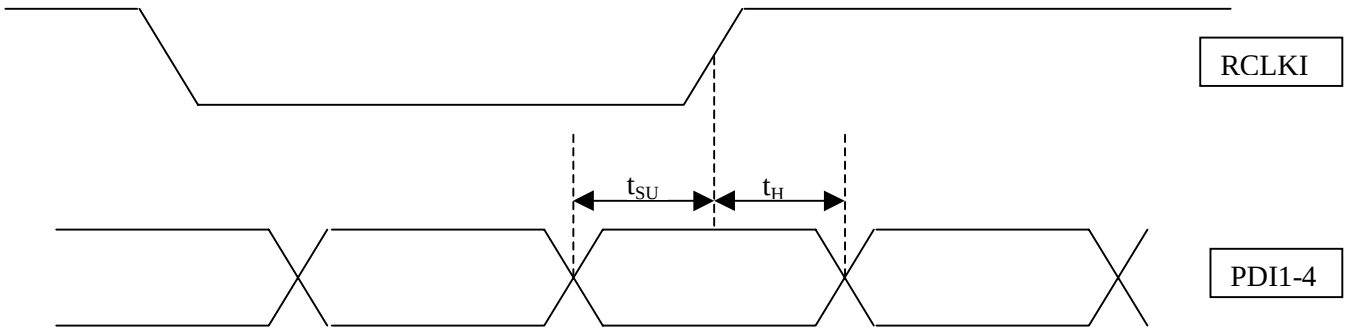
Figure 2. Frame detection/channel assignment disabled, with no inverted outputs at demultiplexer

timing required to ensure that data is aligned during multiplexing. The rising edge of RCLKI is *the first rising edge of RCLKI after RSETES has been reset.*

(See the timing diagram shown in the figure below.)

Note that t_{SU} is defined as time before the rising clock edge. The negative value for t_{SU} means that the setup time comes after the clock edge, so the data must not transition between 200ps to 600ps after the clock edge.

For this discussion to be valid, the requirements of the elastic store block must be met. The elastic store block requires that data be valid on the inputs for 10µs before a reset pulse of at least 10ns is applied to RSETES.



t_{SU} = -200ps
t_H = 600ps